

COUNTER-BASED PHASE SHIFTER CIRCUITS AND METHODS WITH
OPTIONAL DUTY CYCLE CORRECTION

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ABSTRACT

Phase shifter circuits and methods use counters to define the positions of the output clock edges. A plurality of counters are each clocked by a count clock relatively much faster than the input clock. A first counter counts for one input clock period, and a delay value is determined based at least in part on the counted value. In some embodiments, the delay value has a maximum value that depends on the counted value. The delay value is provided to a second counter, which counts from zero to the delay value and generates a pulse one delay value after the beginning of the input clock period. A third counter running at the same clock rate generates a pulse after an additional delay. The pulses from the counters are used to provide output clock edges at predetermined times during the input clock cycle. Some circuits also perform a duty cycle correction.